

FIG. 1

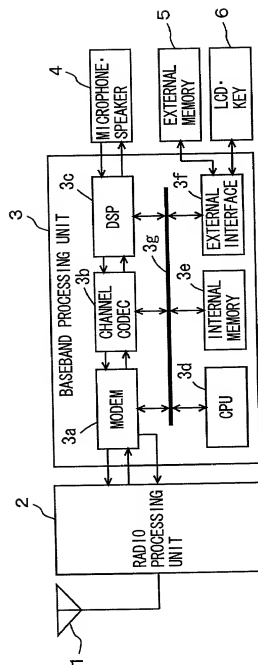


FIG. 2

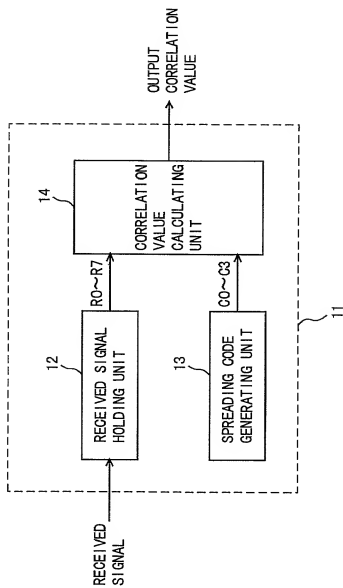


FIG. 3

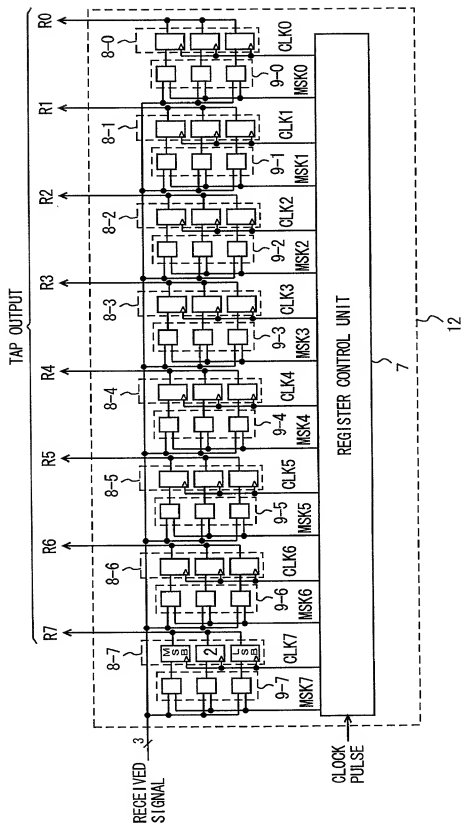


FIG. 4

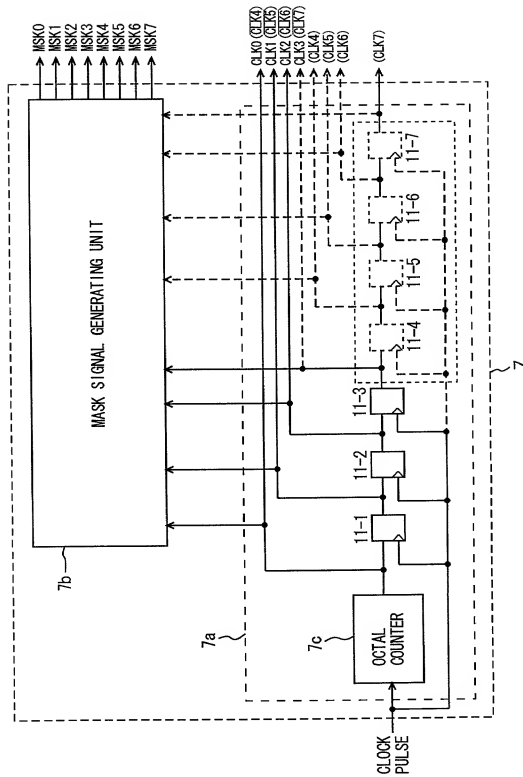


FIG. 5

	INPUT SIGNAL				OUTPUT SIGNAL							
	CLK3	CLK2	CLK1	CLK0	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0
(1)	L	L	L	L	1	1	0	0	0	0	0	0
(2)	L	L	L	H	0	1	0	0	0	0	1	0
(3)	L	L	H	L	1	0	0	1	0	0	0	0
(4)	L	L	H	H	0	0	0	1	0	0	1	0
(5)	L	H	L	L	0	1	1	0	0	0	0	0
(6)	L	H	L	H	0	1	0	0	1	0	0	0
(7)	L	H	H	L	0	0	1	1	0	0	0	0
(8)	L	H	H	H	0	0	0	1	1	0	0	0
(9)	H	L	L	L	1	0	0	0	0	0	0	1
(10)	H	L	L	H	0	0	0	0	0	0	1	1
(11)	H	L	H	L	1	0	0	0	0	1	0	0
(12)	H	L	H	H	0	0	0	0	0	1	1	0
(13)	H	H	L	L	0	0	1	0	0	0	0	1
(14)	H	H	L	H	0	0	0	0	1	0	0	1
(15)	H	H	H	L	0	0	1	0	0	1	0	0
(16)	H	H	H	H	0	0	0	0	1	1	0	0

FIG. 6

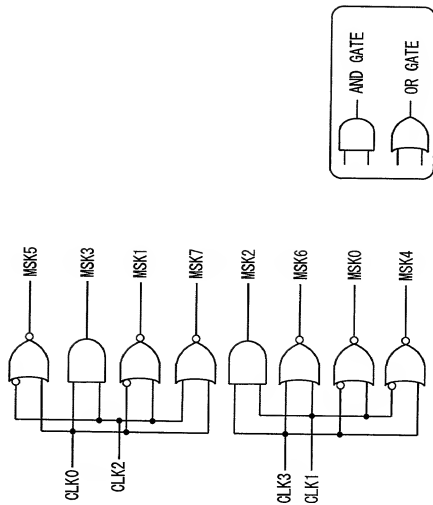


FIG. 7

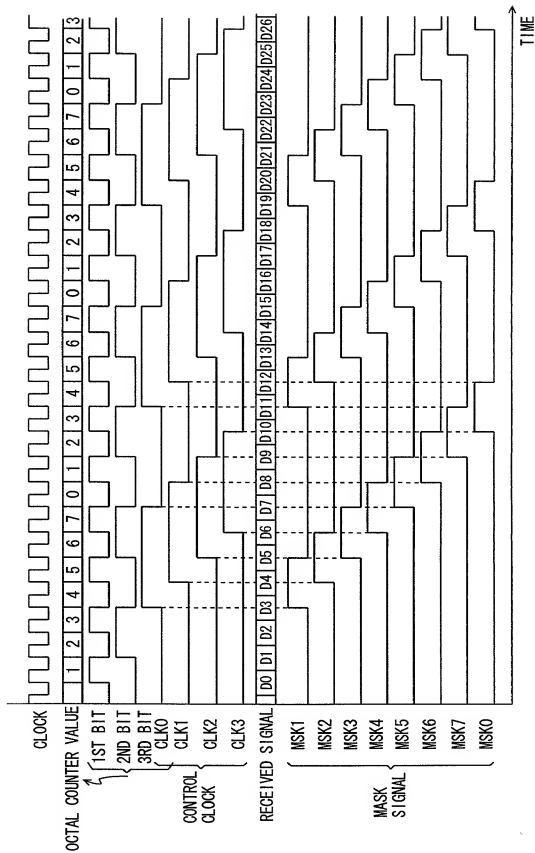


FIG. 9

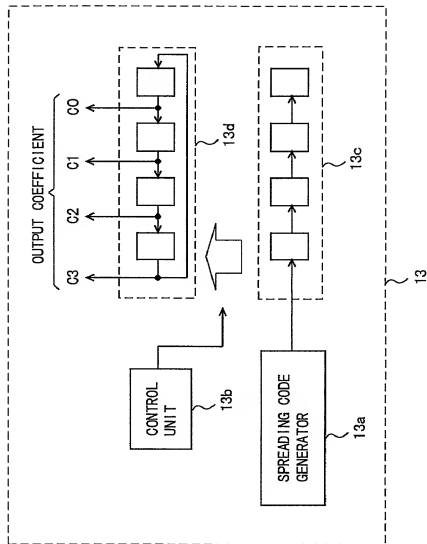


FIG. 10

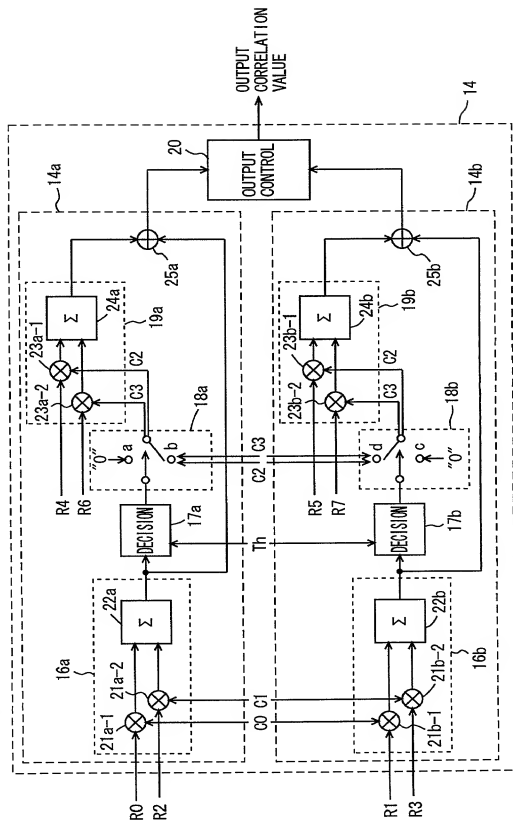


FIG. 11

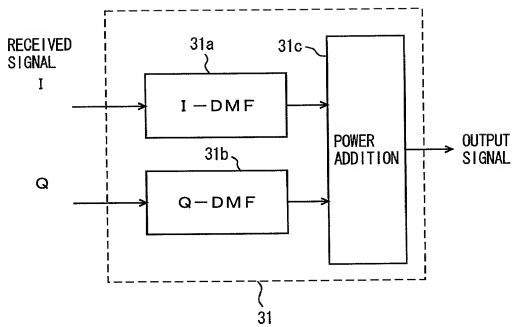


FIG. 12A

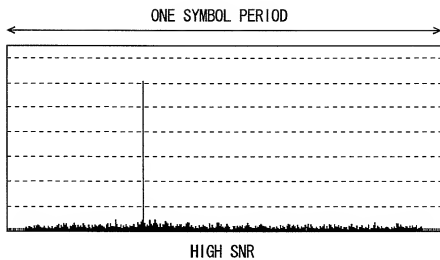
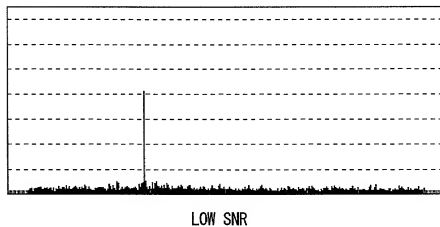


FIG. 12B



009221.96654760

FIG. 13

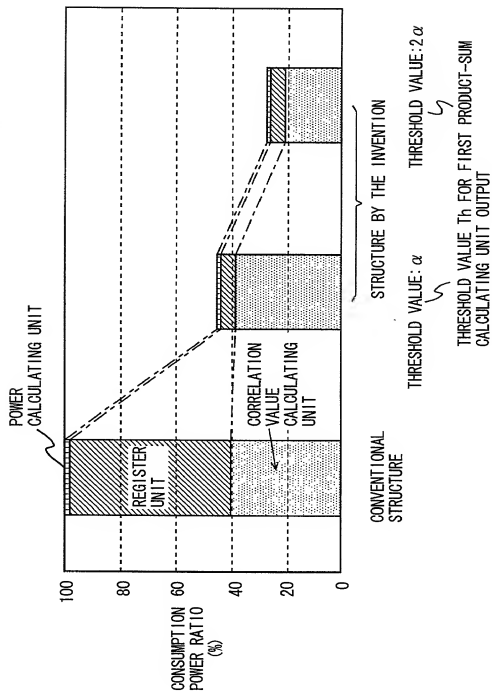


FIG. 14 PRIOR ART

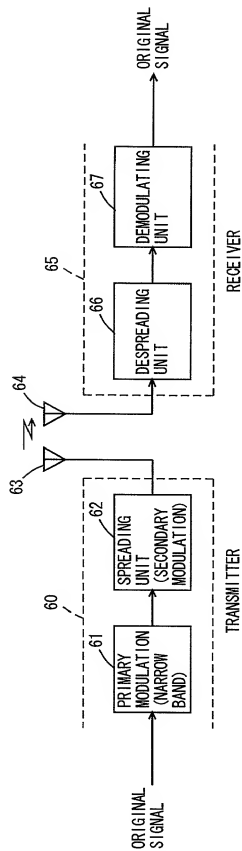


FIG. 15 PRIOR ART

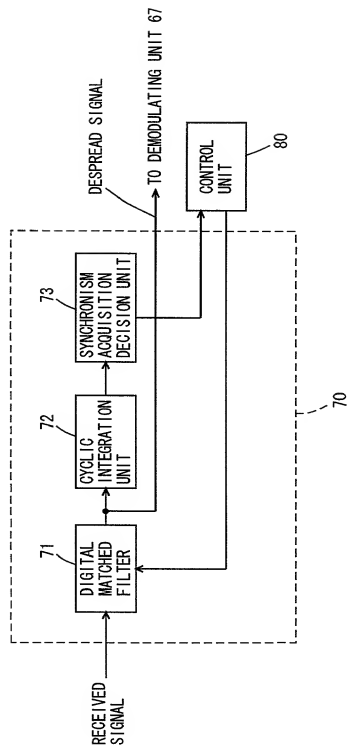


FIG. 16 PRIOR ART

